A 0.5 V, 420 MSps, 7-bit Flash ADC Using All-Digital Time-Domain Delay Interpolation

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***Abstract*—This paper presents a 0.5 V ultra-low-voltage flash ADC using an all-digital time-domain delay interpolation technique for resolution enhancement. The developed 7-bit flash ADC is implemented in a 90 nm CMOS process. By using two-way time-interleaving, it achieves an ENOB of 5.5 bits while operating at 420 MSps consuming a total power of 4.1 mW. The measured peak FoM is 195 fJ/conv.-step during single-channel operation at 210 MSps.**

Keywords-flash ADC; ultra-low-voltage; delay interpolation

I. INTRODUCTION

High-speed, low-resolution, ultra-low power ADCs are strongly required for DVD and portable applications. In addition, such low-resolution, low-latency ADCs are crucial building blocks for the development of higher resolution ADCs such as delta-sigma ADCs, sub-ranging ADCs, and pipeline ADCs.

This paper presents an ultra-low-voltage flash ADC using an all-digital time-domain delay interpolation technique [1] to enhance its resolution without compromising its power performance. The 7-bit flash ADC fabricated in 90 nm CMOS realizes 420 MSps operation through two-way time-interleaving while consuming only 4.1 mW from a 0.5 V supply. The achieved ENOB is 5.5 bits. An ultra-low figure of merit (FoM) of 195 fJ/conv.-step has been attained during single-core operation.

II. CIRCUIT DESIGN

A. All-Digital Time-Domain Delay Interpolation Technique

The time-domain delay interpolation compares the delays of two adjacent dynamic comparators, where the intersection of the two comparators' delays is the interpolation point, as illustrated in Fig. 1. By analyzing the delays, we can extract additional information to further quantize the input signal because the signal is always closer to the comparator with a longer delay due to the effect of metastability. Fig. 1 also shows the schematic of the all-digital time-domain delay interpolation technique implemented using only digital SR latches.

B. Mismatch Compensation by Variable Capacitance

This ADC uses MOM capacitors that are better suited for scaled CMOS technology instead of the commonly used varactors [2] for its calibration. The calibration circuit is shown in Fig. 2, where the digitally-controlled variable capacitance acts as the load for the dynamic preamplifier circuit in a dynamic double-tail latched comparator [3].

C. Overall Design of ADC

Fig. 3 shows the 6-bit ADC core, which consists of the 5-bit ADC core from [4] implemented with the proposed delay interpolation. Fig. 4 shows the overall block diagram of the ADC presented in this paper. This ADC contains two 7-bit ADC cores that are realized by summing four 6-bit ADC cores. To reduce the added delay due to ultra-low-voltage operation, two 7-bit ADC cores are time-interleaved to obtain high-speed operation.

III. EXPERIMENTAL RESULTS

From measurement results, a 0.5 V ultra-low-voltage operation has been attained with a high conversion frequency of 420 MSps while only consuming 4.1 mW. Fig. 5 (a) shows the signal to noise and distortion ratio (SNDR) and spurious free dynamic range (SFDR) versus the conversion rate when the input signal is about 1 MHz with a 0.5 V supply voltage. Fig. 5 (b) shows an effective resolution bandwidth (ERBW) of 50 MHz and 200 MHz for the interleaved and single core ADCs, respectively. This ADC is fabricated using a 90 nm CMOS technology with the deep N-well and low threshold voltage options occupying a total area of 0.39 mm^2 as shown in Fig. 6. The performance summary is presented in Table I along with other relevant state of the art ADCs.

IV. CONCLUSION

In this paper, a 0.5 V ultra-low-voltage, 7-bit, 420 MSps flash ADC using an all-digital time-domain delay interpolation technique for resolution enhancement and a MOM variable capacitance calibration technique is presented. The measured results show high speed performance while consuming only 4.1 mW from a 0.5 V supply.

ACKNOWLEDGMENT

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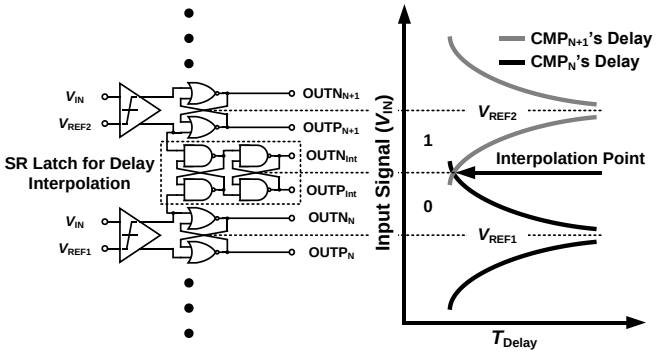

Figure 1. The all-digital time-domain delay interpolation schematic.

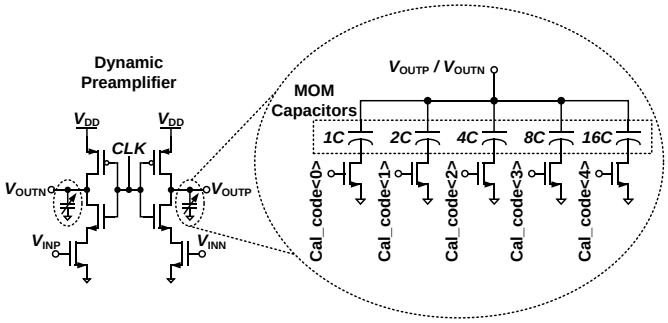

Figure 2. A variable capacitance calibration circuit using MOM capacitors and switches.

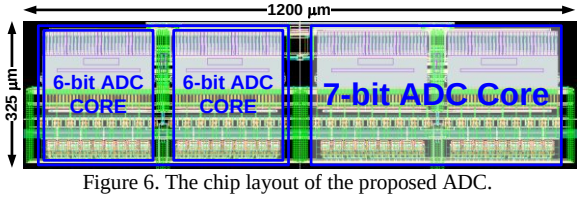

Figure 6. The chip layout of the proposed ADC.

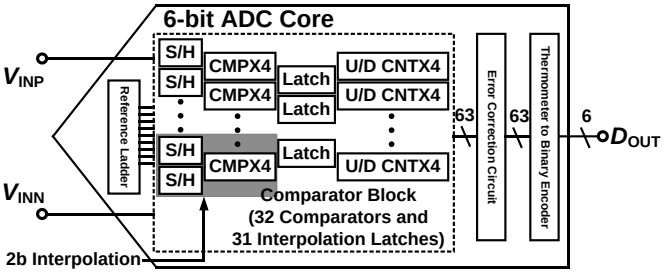

Figure 3. The 6-bit ADC core with the proposed all-digital time-domain delay interpolation technique and gate-interpolation technique.

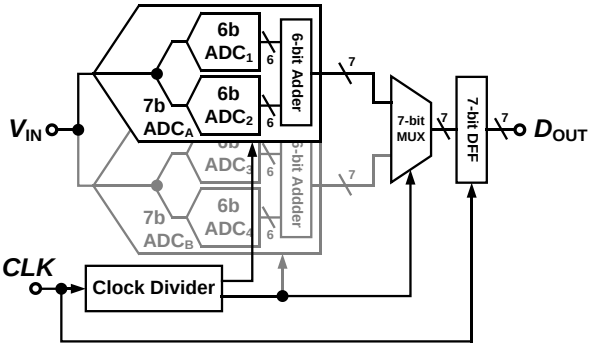

Figure 4. The overall ADC block diagram showing the two 6-bit ADC cores summed together to realize the 7-bit ADC core, which is then used to implement two-way time-interleaving to obtain the high-speed performace with a 0.5 V supply.

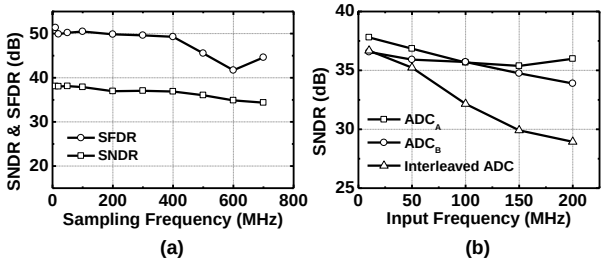

Figure 5. (a) shows the ADC's SNDR and SFDR vs. conversion frequency for 0.5 V with 1 MHz input signal and (b) shows the ERBW of two single cores and the interleaved ADC with a conversion frequency of 210 MHz and 420 MHz, respectively.

TABLE I. STATE OF THE ART PERFORMANCE COMPARISON

	[5]	[6]	[7]	This Work	
Architecture	Subrange	Subrange	Pipeline	Flash	
Resolution [bit]	7	7	10	7	
f_s [MSps]	2200 (4 ch)	300 (1 ch)	10 (1 ch)	420 (2 ch)	210 (1 ch)
Process [nm]	65	65	90	90	
Supply [V]	1	1.2	0.5	0.5 (V_{BS} = 0.5)	
SNDR [dB]	36.1	40.5	48.1	35	36
Power [mW]	40	2.3	2.4	4.1	2.1
FoM [fJ/c.-s.]	280	88	940	906	195